

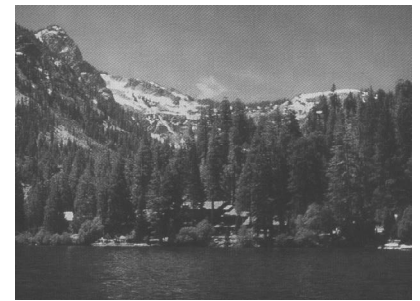


1996 International

INTEGRATED RELIABILITY WORKSHOP

October 20-23, 1996

<http://www.irps.org/irw/>



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WORKSHOP EXPERIENCE

You are cordially invited to participate in the 1996 Integrated Reliability Workshop. The Workshop provides a unique forum for sharing new approaches to achieve and maintain microelectronic component reliability. The Workshop features presentations, tutorials, open poster sessions, moderated discussion group sessions, and special interest group (SIG) meetings. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing.

MAJOR TECHNICAL THEMES

Aggressive cost, reliability, and market entry demands are forcing the semiconductor industry to consider alternatives to the traditional and increasingly inadequate approach of testing-in-reliability (e.g., burn-in, life test). In response to these concerns, the Workshop is continuing to highlight the need for an integrated approach to ensure product reliability, in which a detailed understanding of potential failure mechanisms and their sources are proactively incorporated into robust design and manufacturing practices. The four topical areas for this year's Workshop reflect the scope of this approach and serve as a framework for exploring solutions.

- **PHYSICS OF THE FAILURE** — Fundamental investigations into potential failure mechanisms, their sources, and methods of activation.
- **RELIABILITY TEST STRUCTURES** — Tools for investigating and monitoring failure mechanisms.
- **WAFER LEVEL RELIABILITY** — In-line or end-of-line reliability measurements for manufacturing control verification and early detection of specific reliability problems.
- **BUILDING-IN RELIABILITY** — A methodology for eliminating causes of product failure through proactive reliability engineering integrated throughout all phases of product conception, development, and manufacturing.

(over)

ExOfficio Members & IRPS Board Representatives

Harry A. Schafft
NIIST

Patrick E. Kennedy
McDonnell Douglas

PROGRAM ANNOUNCEMENT!

'96 Workshop Features:

- ★ 20+ Technical Presentations on:
 - Physics of Failure
 - Reliability Test Structures
 - Wafer Level Reliability
 - Building In Reliability
- ★ Keynote Address: **Does Building-In Reliability Imply More or Less Wafer-Level Reliability Testing?**
Joe McPherson, Ph.D, TI Fellow
Texas Instruments, Inc., Dallas, Texas
- ★ Tutorials
 - Predictive WLR: A New Archetype
 - Metallization Reliability
- ★ Group Discussions
 - WLR Techniques as a Q & R Tool
 - BIR Implementation
 - Interconnect Reliability
 - Thin Oxide Reliability
- ★ Open Poster Sessions
- ★ Special Interest Groups

IEEE/Integrated Reliability Workshop
P.O. Box 308
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KEYNOTE: DOES BUILDING-IN RELIABILITY IMPLY MORE OR LESS WAFER-LEVEL RELIABILITY TESTING?

Joe McPherson, Ph.D, TI Fellow
Texas Instruments, Inc., Dallas, Texas

Wafer-level reliability (WLR) testing continues to be an important tool for implementing a building-in reliability (BIR) strategy. The thrust of WLR testing has shifted, however, from the back of the line (monitoring of outgoing reliability levels) to the front of the line (margin testing during the development and productization phase). The rapid nature of most WLR tests permits the process engineer to evaluate the impact of process variation and to obtain an “almost instantaneous” feedback as to its reliability impact. Rapid reliability feedback is a key to helping the process engineer to build reliability into the technology. This is extremely important today when technologies are being developed and introduced to fabs at a rapid rate.

DISCUSSION GROUPS

A highlight of the Workshop is the evening discussion group program. Attendees will have a choice of four topics on both Monday and Tuesday evenings. The same four topics will be discussed for 90 minutes each night. This year's topics are:

WAFER LEVEL TECHNIQUES AS A QUALITY AND RELIABILITY TOOL

Leaders: Don Pierce and Eric Snyder, Sandia Technologies

The large stresses used in wafer level reliability test techniques yield data with test times orders of magnitude shorter than conventional techniques. These fast tests have drawn much interest throughout the industry, though there appears to be tremendous variability in implementation, approach, and application.

In this discussion group, group participation will be used to scope the degree of implementation of WLR across the industry, what new requirements could be met by WLR and what advances in WLR techniques are needed to meet those requirements.

BIR IMPLEMENTATION DISCUSSION GROUP

Leaders: James Prendergast and John Steeves, Analog Devices

BIR is a proactive approach to reliability, where it must be recognized that the end goal of a company is to produce reliable product in a timely, cost-effective manner. This can be done now only if reliability is incorporated into the design, process, and assembly phases of product development. While we all, I think, agree that this is the correct approach to adopt — implementation of BIR is not easy because it requires, among other things, rather severe changes in attitude and in traditional working relationships.

You all, novices to experts, come to this discussion group to share your experiences, data, questions, perspectives as we — in lively, interesting and entertaining discussions — seek to discover and to describe paths of BIR implementation.

INTERCONNECT RELIABILITY

Leaders: Tim Sullivan, IBM and Shekhar Pramanick, AMD

Suggested topics for discussion:

- Can wafer level testing techniques provide valid and accurate lifetime projection, or do current and temperature levels fundamentally alter electromigration physics, kinetics or failure localization?
- How do refractory layers affect lifetime?
- Can wafer level techniques be used to evaluate their effectiveness?
- Does stress voiding influence wafer level EM more or less than conventional EM testing?
- Are thermal gradients more important in wafer level testing?
- Can results be invalidated by neighboring structures such as W studs?

THIN OXIDE RELIABILITY

Leaders: John Suehle, NIST and Raif Hijab, AMD

Suggested topics for discussion:

- What information do wafer level oxide evaluation tools (Vramp, Qbd, etc.) provide?
- What's hot in new oxide evaluation methods, particularly for very thin oxides?

- How useful are they for reliability prediction?
- What test conditions and breakdown criteria are applicable for very thin oxides?
- What is the validity of oxide reliability models at high & low fields?
- What is the upper temperature limit for valid extrapolation to lower temperatures?
- How is oxide thickness accurately determined from measurements (CV, FN, etc.)?
- What corrections are needed for calculating the actual field across the oxide?

TUTORIALS

In our continuing effort to enhance the value of the Workshop and to strengthen the Technical Program, we are again offering two tutorials on Sunday afternoon.

PREDICTIVE WAFER LEVEL RELIABILITY: A NEW ARCHETYPE—Don Pierce and Eric Snyder, Sandia Technologies

Assuring IC reliability is becoming more of a challenge as device geometries shrink, environments become more stressful and the time-to-market becomes shorter. Traditional wafer level reliability (WLR) approaches have emphasized test speed over quality of data with the underlying assumption that WLR at best is a crude indicator of process reliability. We believe that if sound physical principles are followed, the quality of WLR data can be improved dramatically and can yield results identical to those obtained using much slower and more costly packaged-test approaches. This is a dramatic departure from the conventional wisdom and is steeped in controversy, as is often the case with the state-of-the-art.

We will describe how implementation of this new type of WLR helps semiconductor manufacturers and users meet the challenge of assuring IC reliability. This physics-based approach provides quantitative data economically in a short period of time, supporting process monitoring, rapid reliability qualification of processes/foundries and extraction of key parameters that will be needed for future design for reliability tools. This tutorial will show the approaches needed to maximize the quality of WLR data using theory backed up with data. The technical examples will demonstrate the features and utility of WLR when the test methodology optimized for predictability and not just speed. This, the proper approach to WLR, saves time and money over traditional WLR.

EFFECTS OF MECHANICAL STRESSES, MICROSTRUCTURE AND INTERCONNECT STRUCTURE ON METALLIZATION RELIABILITY—John Sanchez*, University of Michigan and Paul Besser, Advanced Micro Devices (*presenter)

It is well known that stresses, microstructure and the structure of metallization interconnects controls the reliability of patterned interconnects in integrated circuit devices. This tutorial will review some of the fundamentals in each of these areas, and provide a connection between fundamental understanding and applied interconnect engineering issues for both development and manufacturing environments. Actual examples which are useful for the design of more manufacturable and more reliable interconnect systems will be presented.

Deposited metal films and patterned lines are often subjected to large stresses and strains. The nature of these stress states, which is determined by the film or line geometry, will be reviewed. The metallurgical and geometrical factors which control the mechanical behavior of films and lines are presented, as are the processes which induce hillocks, sunken grains and voids.

The next part of this tutorial will focus on the microstructural evolution of metal films and lines, and review these effects on electromigration-induced failure mechanisms. The effects of line grain size and textures on reliability will be presented, including theoretical calculations, simulations and correlations with experimental results.

The effects of layering Al with refractory barriers on interconnect microstructure and reliability will be discussed. Control of the Al microstructure (grain size and texture) by the correct choice of Ti and/or TiN layering schemes for improved performance, manufacturing reliability and performance will be discussed. It will be shown that the Ti + Al reaction can be controlled by the proper choice of Al-alloy.

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(continued from page 2)

OPEN POSTER SESSIONS

The Technical Program will include two open poster sessions. All attendees have the opportunity to present a poster to communicate their ideas and results on a technical project or issue. There is a place on the registration form to reserve a poster display board (32" × 40" or 81 cm × 100 cm). Your work should be in Landscape format on 8 1/2 × 11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a one-page abstract of your poster presentation for inclusion in the Workshop Final Report. This is a great opportunity for you to share your work with your peers.

SPECIAL INTEREST GROUPS (SIG)

The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information about SIGs is encouraged to contact SIG Coordinator, David Kirchner at dwk@smtmhs.sharpwa.com.

JEDEC 14.2 MEETING

The JEDEC 14.2 Wafer Level Reliability Standards Committee meeting will be held immediately after the workshop at the Stanford Sierra Camp

Wednesday afternoon and Thursday until noon. Members, alternates, and guests are also welcome. Please use the workshop registration form to register for the JEDEC meeting.

MORE INFORMATION

We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical program. If you have any questions, *please contact me*, James W. Miller, by phone, 512-933-7297, or fax, ...7662, or e-mail: rvkg60@email.sps.mot.com, or Cleston Messick, General Chair, at 801-562-7546, fax...7500, email: CCRMSL@tevm2.nsc.com.

REGISTER NOW!

Complete and mail the enclosed registration form. Please register early. We were completely sold out last year. Space at the Camp limits the Workshop to roughly 120 attendees.

We look forward to seeing you at the '96 Workshop!

Sincerely,
James W. Miller
Technical Program Chair

TAHOE CASINO EXPRESS

The Tahoe Casino Express runs from 6:15 a.m. to midnight, every hour from 8:15 a.m. to 3:15 p.m. and every 2 hours before 8:15 a.m. and after 3:15 p.m.. The Tahoe Casino Express charges \$17.00 per person. For more information regarding the Reno/Horizon shuttle service, call 800-446-6128. Stanford Sierra Camp offers courtesy transportation to its guests from the casino to Stanford Sierra Camp. Stanford Sierra Camp must be notified of shuttle service requests at least one week in advance of arrival date (916-541-1244). Pick-up is available from 10:00 a.m. to 10:00 p.m. on the first day of the Workshop. Please notify Camp with your anticipated arrival time at the Horizon Casino. Return trips are offered on the last day of the Workshop only. In addition, the IRW will provide limited, emergency shuttle service from the Horizon's Casino to the Stanford Sierra Camp. If you find yourself stranded, please call 800-656-6346, PIN 2684.



1996 *International* INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

SUNDAY, October 20

- 2:00 p.m. Early Check-In for *Tutorial* Attendance (pick up badges & handout)
- 3:00 p.m. Regular Check-In (pick up badges & handout)
- 3:00 p.m. Tutorial Sessions
- Predictive Wafer Level Reliability: A New Archetype—Don Pierce and Eric Snyder, Sandia Technologies
 - Effects of Mechanical Stresses, Microstructure and Interconnect Structure on Metallization Reliability—John Sanchez*, University of Michigan and Paul Besser, Advanced Micro Devices (*presenter)
- 5:00 p.m. Mixer and Poster Session (Poster Session Coordinator: Marty Frary, Storage Technology)
- 6:00 p.m. Dinner
- 7:30 p.m. Introduction and Announcements
- 7:45 p.m. Keynote Does Building-In Reliability Imply More or Less Wafer-Level Reliability Testing?—Joe McPherson, Texas Instruments
- 8:45 p.m. Mixer and Poster Session (Poster Session Coordinator: Marty Frary, Storage Technology)

MONDAY, October 21

- 7:00 a.m. Breakfast (until 8:00 a.m.)
- 8:15 a.m. Technical Presentation Session: Building In Reliability, Harry Schafft, NIST, Chair
- BIR-1 BIR - Breaking Down the Barriers—J. Molyneaux, N. Finucane, J. Prendergast, and S. Houlihan, Analog Devices
- BIR-2 The Application of a Direct Parameter Extraction Strategy to Hot-Carrier Reliability Simulation of n-Channel LDD MOSFETs—S. Minehane, A. Meehan, P. O'Sullivan, and A. Mathewson, NMRC Cork Ireland, and B. Mason, GEC Plessey
- BIR-3 The Nanoscilloscope: Simultaneous Topography and AC Field Probing with a Micromachined SFM Tip for Building In Reliability—D. W. van der Weide and P. Neuzil, University of Delaware
- BIR-4 Shear Test for Adhesion Measurement of Small Structures—G. Schammler, K. Buschick, R. Hahn, and H. Reichl, Technische Universität Berlin
- BIR-5 Electrical Characteristics of Wedge-Shaped Gate-Oxide Breakdown—Y.T. Woo, C.-S. Hwang, S.-T. Hong, and I.-S. Chung, Hyundai
- BIR-6 Predicting Oxide Reliability From In Line Process Statistical Reliability Control—J. Prendergast, Analog Devices and E. Murphy and M. Stephenson, University of Limerick
- 12:15 p.m. Lunch
- 2:00 p.m. Technical Presentation Session: Reliability Test Structures, Bruce Aldridge, Motorola, Chair
- BIR-7 (Invited) Process Sensors, Simulation, and Control to Build In Reliability—Gary W. Rubloff, University of Maryland
- RTS-1 A Test Structure for Plasma Process Charging Monitoring for Advanced CMOS Technology—S.U. Kim, SEMATECH
- RTS-2 A VCO Test Structure for Characterizing AC Hot-Carrier Degradation—N. Koike and K. Tatsuma, Matsushita Electronics Corporation
- RTS-3 Is BPSG an Effective Na⁺ Barrier? - A WLR Success Story—J. Schideler, M. Ivey, J. Finn, and C. Messick, National Semiconductor
- RTS-4 (Invited) Test Structures for Rapid Prototyping of Gas and Pressure Sensors—Martin Buehler and Li-Jen Cheng, Jet Propulsion Laboratory and Dennis Martin, Halcyon Microelectronics
- 6:00 p.m. Dinner
- 7:30 p.m. Discussions Groups (90-minute parallel sessions for each topic): Attendees are to participate in one of the four groups.

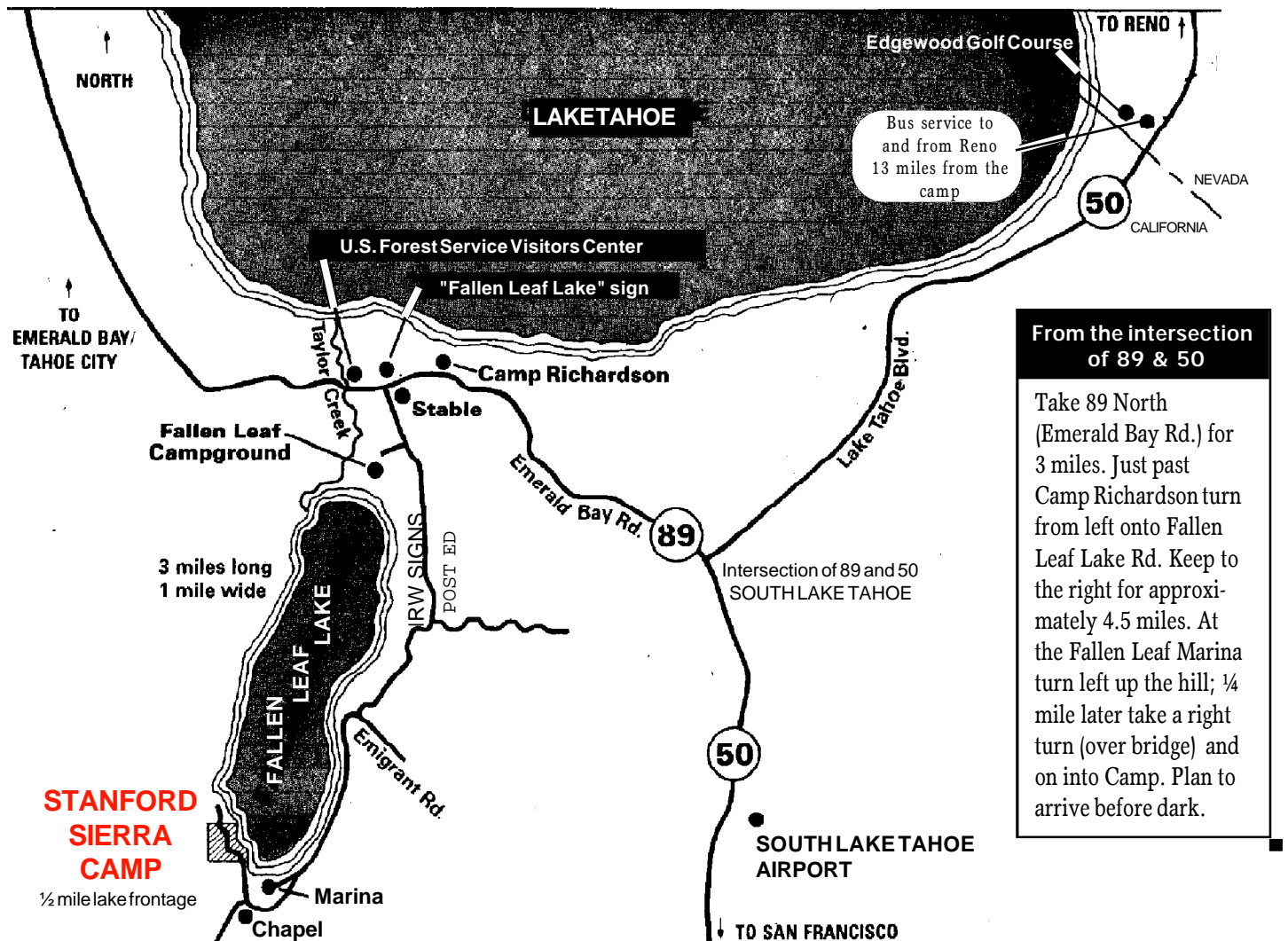
TUESDAY, October 22

- 7:00 a.m. Breakfast (until 8:00 a.m.)
- 8:15 a.m. Technical Presentation Session: Wafer Level Reliability—Jay Shideler, National Semiconductor, Chair
- WLR-1 Wafer Level Reliability Application to Manufacturing of High Performance Microprocessor—K. Sarma, M. Bahrami, and K. Mistry, Digital Equipment Corporation
- WLR-2 Step By Step Method for the Elimination of Burn-In as a Necessary Screen—T. Turner, Keithley Instruments
- WLR-3 Temperature-Constant BT Tests of Parasitic MOSFETs—H. Katto, Science University of Tokyo
- WLR-4 Reverse Antenna Effect Due to Process-Induced Quasi-Breakdown of Gate Oxide—J. Chen, C Gelatos, P. Tobin, and R. Shimer, Motorola, and C. Hu, U.C. Berkeley
- Technical Presentation Session: Physics of Failure—Mark Poulter, National Semiconductor, Chair
- POF-1 Thermal Analysis of the Fusion Limits of Metal Interconnect under Short Duration Current Pulses—K. Banerjee, S. Rzepka*, A. Amerasekera, C. Hu, UC Berkeley, *Texas Instruments
- POF-2 Response of Aged Line/Stud Structures to Stepped Current Stressing—S. Yankee, T. Sullivan, G. Endicott, and W. Klaasen, IBM Microelectronics
- POF-3 Temperature Ageing as a Means of Improving the Electromigration Performance of an Aluminium-Copper Alloy Metallization—S. Foley, D. Martin, and A. Mathewson, NMRC

- 12:15 p.m. Lunch and then... * * * * * *The Afternoon is free for discussion, hiking, and other recreation.* * * * * *
- 5:00 p.m. Open time for SIG meetings (optional)—Coordinator: David Kirchner, Sharp Microelectronics
- 6:00 p.m. Dinner
- 7:30 p.m. Discussion Groups (90-minute sessions for each topic) Attendees are to participate in one of the four groups.

WEDNESDAY, October 23

- 7:00 a.m. Breakfast (until 8:00 a.m.)
- 8:15 a.m. Technical Presentation Session: Physics of Failure (continued)
 - POF-4 Impact of Boron Penetration at the p⁺-Poly/Gate Oxide Interface on the Device Reliability of Deep Submicron CMOS Logic Technology—D. Nayak, M. Hao, and R. Rakkhit, Advanced Micro Devices
 - POF-5 Hole Trapping as the Rate-Limiting Factor in LDD nMOSFET Degradation—A. Gupta, D. Sugiharto, and C. Yang, Santa Clara University, N. Matsuzaki, M. Minami, T. Yamanaka, and T. Nagano, Hitachi
 - POF-6 Effects of N₂O or NO Annealing of Wet Oxide at Different Times on TDDDB Characteristics—M. Mazumder, A. Teramoto, K. Kobayashi, M. Katsumata, Y. Mashiko, M. Sekine, H. Koyama, and A. Yasuoka, Mitsubishi
 - POF-7 Physically Based Predictive Model of Oxide Charging—J. Conley, Dynamics Research Corp. and P. Lenahan and B. Wallace, Penn State University
 - POF-8 Injected Charge as an Indicator for a t_{bd} Increase of Pre-Stressed Gate Oxides—A. Martin, P. O'Sullivan, T. Ribbrock*, and A. Mathewson, NMRC Cork Ireland *RWTH Aachen Germany
 - POF-9 Thickness and Temperature Effects on TDDDB for DC and Dynamic Stressing of Thin Oxide—S.-H. Soh, National Semiconductor and M. Naidu, J. Hwu, and L. Sadwick, University of Utah
- 11:40 a.m. Closing Remarks
- 12:15 p.m. Lunch and then leave the Stanford Sierra Camp unless attending JC14.2
- 2:00 p.m. EIA/JEDEC Committee 14.2 Wafer Level Reliability Meeting, Michael Dion, Chair (mdion@harris.com)



RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ARRANGEMENTS INFORMATION

AIR TRAVEL GROUP RATES: The IEEE/EDS has arranged for Group rates with **United Airlines:** 5% off the lowest available fare. Call 1-800-521-4041 to check restrictions and fares. Provide United with the Meeting ID Number: 587NP.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- **The 1996 IRW is providing shuttle busses from Reno International Airport to the Stanford Sierra Camp.** The **IRW shuttle** will depart Reno International Airport at 12:00 noon, 2:30 p.m., and 4:30 p.m. local time on Sunday, October 20. Reservations will be accepted. You may make reservations by leaving a voice mail message for Doug Menke at 512-933-2491, or by FAX 512-933-2164 or, by email at ra4864@email.sps.mot.com. Any remaining seats will be available on a first come, first served basis. At the conclusion of the Workshop the IRW shuttle busses will leave the Stanford Sierra Camp for the Reno International Airport at 1:30 p.m. on Wednesday, October 23 (following the Workshop), and at 1:00 p.m. on Thursday, October 24 (following the JEDEC meeting).
- Transportation is also available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the **Tahoe Casino Express**. For **Tahoe Casino Express** schedule details see the other side of this page.

ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking will not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3971.
- A message board will be available for incoming calls, (916) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



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1996 IRW REGISTRATION FORM

(Please type, print clearly, or attach business card)

(Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 23-24)

REGISTRATION FEES (US\$)

NAME: _____ TITLE: _____
Last First Initial
 COMPANY: _____ Mail Code _____
 ADDRESS: _____
City State/Country Zip/Postal Code
 PHONE: (_____) _____ FAX: _____
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IEEE Member _____ .. **\$875*** _____
(member No. Req'd)
 NON-IEEE Member **\$950*** _____
 * Includes meals, lodging, Handout, & Final Report.
(Sun. eve., Oct. 20- Wed. noon, Oct. 23)
 EXTRA COPIES of Workshop
 Final Report Qty: _____ x **\$80** _____
 JC14.2 accommodations **\$160†** _____
TOTAL REMITTED \$ _____

- Address is HOME, Company not to be included on mailing label
 - Please check here if you do not wish to receive mail other than from IRW & IRPS
 - Please check here if under the Americans With Disabilities Act, you require any auxiliary aids or service. Please call (315) 339-3971.
- For rooming assignments, please check one: male female

Meeting registration automatically includes a room reservation.

SORRY, WE DO NOT TAKE CREDIT CARDS

- MAKE CHECKS PAYABLE TO "IEEE INTEGRATED RELIABILITY WORKSHOP"
- Wire Transfer: Marine Midland Bank, 853 Black River Blvd., Rome, NY 13440; Acct. name: IEEE/IRW 1996; Acct. #: 192453297; ABA #: 021001088

Each Attendee will only attend one Discussion Group each night. Please Indicate your Discussion Group Preference

Mon	Tues.	Discussion Group Topic
		WLR Techniques as a Q & R Tool
		BIR Implementation
		Interconnect Reliability
		Thin Oxide Reliability

SEND PAYMENT & FORM TO:

IEEE IRW
 P.O. Box 308
 Westmoreland, NY 13490

For registration information:
 phone: 315-339-3971
 FAX: 315-336-9134
 email: sar@ntcnet.com

- WILL
- WILL NOT ATTEND SUNDAY TUTORIALS (3-5 p.m.). If you plan to attend, please indicate preference for topic below:
- Predictive WLR: A New Archetype
- Metallization Reliability

YOUR POSTER TITLE: _____

You will be provided with a poster board for one of the poster sessions to share your ideas and your results on a technical topic or issue. Instructions will be sent to you if you register for a poster. You will be provided with a 32" x 40" poster board.

*The Workshop Registration Fee includes: your housing accommodations at the Stanford Sierra Camp cabins, all meals and refreshments (no-host bar), on-site recreation activities, parking for your car, the Presentation Viewgraph Booklet (at the workshop), and the Final Report (after the workshop).

† The JEDEC Committee fee for accommodations includes: housing on Wednesday night, meals (from dinner on Wednesday through buffet lunch on Thursday), refreshments, and parking for your car.

CANCELLATION fees: \$50 AFTER SEPTEMBER 26; FULL FEE AFTER OCTOBER 10