IEEE/Integrated Reliability Workshop
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PROGRAM ANNOUNCEMENT!

You are cordially invited to participate in the 2005 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and helpful discussions. You should come away from the workshop intellectually stimulated and with new and refreshed contacts with colleaques.

Major Technical Themes

As the industry aggressively scales towards the limits of materials, reliability is becoming more important than ever, in some areas potentially limiting future performance gains. The Integrated Reliability Workshop deals with a wide and well-balanced spectrum of pressing reliability challenges, preparing attendees for reliability problems at hand as well as those to come. The focus points reflected by this year's program include standard and new gate dielectrics and their reliability impact, NBTI, interconnect, device, and product reliability.

This year's workshop features nine tutorials by world leading experts. Topics include high-k and thin oxide reliability, interconnect reliability, flash memory reliability, reliability statistics, radiation reliability, product reliability, and NBTI. Eight tutorials will be presented in two parallel sessions on Monday afternoon. A ninth tutorial will be presented on Tuesday afternoon. Tutorial abstracts appear in this announcement.

Our keynote, on Tuesday morning, picks up on another important theme: "Status and Future Trends in Technology Reliability: Balancing Technical Challenges and Affordability" - presented by Dr. Erwin Hammerl, Senior Director of Reliability Methodology, Infineon Technologies AG, Munich, Germany.

As usual, all authors, including the tutorial speakers and the keynote speaker will be available for discussions during the workshop. Ample time is scheduled for one-on-one exchanges and for sharing experience and concerns. There will be four organized discussion groups, the popular and productive SIGs (Special Interest Groups), as well as intersession breaks. In addition to 16 refereed posters, another highlight is the open poster sessions, where all attendees are encouraged to display a poster and discuss their most recent (even last-minute) work, ideas, and results. Wednesday afternoon is available for recreation with fellow attendees, a great way to become more acquainted with your colleagues.

Overall this represents an exciting, well-balanced program that addresses the needs and interests of today's reliability engineers for the benefit of their company. We invite you to tell your colleagues and your managers about this year's IIRW. Make a point to let them know that both the attendees and their organizations gain from this investment in learning, which helps in dealing with today's challenges and preparing for tomorrow's.

'05 Workshop Features:

- ✶ **Keynote: Technology Reliability: Balancing Technical Challenges & Affordability—Dr. Erwin Hammerl, Sr. Director of Reliability Methodology, Infineon Technologies**
- ✶ **Group Discussions**
  - Gate Oxide / High-k Reliability
  - NBTI
  - Interconnect Reliability
  - Product/Circuit Reliability
- ✶ **9 Tutorials**
  - Intrinsic Limitations High-k Rel.
  - Flash Memory Reliability
  - Prod Rel.: 90 nm CMOS & Beyond
  - Design-in Rad. Rel. at Comm.Foundries
  - Design-in Rel.– Emphasis on NBTI
  - Reliability Statistics
  - Back End Reliability
  - MEMS Reliability
  - Micro Breakdown to Hard Breakdown—Artifact to Destructive Failure?
- ✶ **22 Technical Presentations on:**
  - Interconnect Reliability
  - Ultra-Thin Oxides / High-k Reliability
  - NBTI
  - Device/Circuit/Product Reliability
- ✶ **16 Refereed Posters + Open Posters**
- ✶ **Special Interest Groups**

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–over–

KEYNOTE

Status and Future Trends in Technology Reliability: Balancing Technical Challenges and Affordability

Dr. Erwin Hammerl, Senior Director of Reliability Methodology, Infineon Technologies AG, Munich, Germany

The ever increasing complexity and performance of semiconductor products in combination with continuous feature size scaling imposes many new reliability challenges (reliability per transistor or per length of interconnect; increasing power and electrical fields, etc). In addition substantial technology changes for the upcoming technology nodes like introduction of new materials, processes, devices and packaging techniques require many additional reliability engineering efforts. Cost of technology development and qualification as well as time to market will be more challenging. Consumer, industrial and automotive applications ('zero defects') with diverging reliability requirements (environmental parameters, accepted failure rates, required life times) are all under cost constraints. Cost optimization requires more accurate lifetime models and new reliability methods, e.g. design for reliability. In this presentation the most critical current and future reliability topics will be highlighted. Levers for reliability cost limitation in technology development and levers for fast time to market, as well as levers for cost efficient reliability monitoring in manufacturing will be discussed.

Tutorials

Chair: Sylvie Bruyere, STMicroelectronics

From Micro Breakdown to Hard Breakdown - from Artifact to Destructive Failure?

Robin Degraeve, IMEC

Tutorial A1, Monday, 1:30-2:30 p.m. (Angora Room)

When a constant voltage stress is applied to a thin (< 10 nm) oxide layer many degradation phenomena are observed: hard breakdown, analog and digital soft breakdown, micro breakdown, progressive breakdown, stress-induced leakage current, anomalous stress-induced leakage current, etc. All of these have in common that they are localized stress-induced leakage paths involving electrical trap centers in the bulk of the oxide, but different names are in use depending on the magnitude of the leakage current or on the application where they are typically measured. Some of these stress-induced leakage paths can be negligible artifacts for one application while they are showstoppers for another application. This tutorial aims at presenting a comprehensive overview of all these dielectric breakdown phenomena, explaining their origin and showing what test methods and structures are needed to observe and study them. Examples will be presented on SiO_2, SiON and some high-k dielectrics.

MEMS Reliability

Danelle Tanner, Sandia National Labs

Tutorial B1, Monday, 1:30-2:30 p.m. (Cathedral Room)

The main thrust in any reliability work is identifying failure modes and mechanisms. This is especially true for the new technology of MicroElectroMechanical Systems (MEMS). This tutorial will include a brief review of MEMS fabrication methods and identify some commercial products. We describe some of the methods developed to measure materials parameters and surface properties to characterize MEMS devices. Our reliability methodology employs statistical characterization and testing to help us identify dominant failure modes. We strive to determine the root cause of each failure mode and to gain a fundamental (science-based) understanding of that mechanism. The development of predictive models follows from this science-based understanding. A reliability model for wear in a MEMS application with contacting surfaces is presented.

Intrinsic Limitations on the Performance and Reliability of High-k Gate Dielectrics for Advanced Electronic Devices

Gerry Lucovsky, NC State

Tutorial A2, Monday, 2:30-3:30 p.m. (Angora Room)

Three different types of high-k thin film oxides have been considered as alternative/replacement gate dielectrics for advanced Si devices for CMOS applications. These are: i) elemental transition metal/trivalent lanthanide rare earth oxides, with the leading candidate being HfO_2, ii) transition metal silicate and aluminate alloys, with the leading candidate being nitrided Hf silicates, and iii) transition metal/rare earth complex oxides, with one of the leading candidates being La aluminate, $LaAlO_3$. Each of these high-k oxide dielectrics is qualitatively different than thermally-grown SiO_2 and/or Si oxynitride alloys that are currently integrated into state-of-the-art CMOS devices, and integrated circuits. This tutorial will address fundamental differences between i) the electronic structure of band edge states in these three different classes of high-k dielectrics with respect to the corresponding band edge states in SiO_2 and Si oxynitride alloys, and ii) thin film stability as it relates to chemical phase separation and/or crystallization of the transition metal silicate and nitrided silicate alloys that occurs at the temperatures required for process integration of CMOS devices and integrated circuits/systems. The intrinsic properties of the candidate high-k alternative gate dielectrics identified above impact primarily on device performance, but are also important with respect to i) process integration, including latitude and yield, and ii) accelerated device testing for projecting device lifetimes such as, for example, the projected time to device and circuit breakdown and failure.

Reliability Engineering Tools: Bootstrapping and Extreme Value Statistics

Larry Stout, Idaho State Univ.

Tutorial B2, Monday, 2:30-3:30 p.m. (Cathedral Room)

This tutorial will provide practical information on two techniques that are of use to anyone doing statistical data analysis and making statistical inferences.

Reliability engineers often base their decisions on fitting lifetime data to a particular type of distribution (e.g. lognormal, exponential, Weibull). Statistical bootstrapping is a tool that allows us to explore data and make useful inferences (e.g. mean, confidence intervals) about it without the need for assuming that the data is from a particular underlying distribution.

To bootstrap a statistic (e.g. the sample mean), we draw for example 1000 random resamples with replacement from the original sample data, calculate the statistic of interest (sample mean) for each resample, then estimate the overall sample mean by taking the average of all the 1000 resampled means. Inferences about our statistic can then be made by inspecting the resulting bootstrap distribution of our 1000 resampled values of the statistic of interest.

The key idea here is that the bootstrap distribution approximates the sampling distribution of the statistic and we use it as a way to estimate the variation in a statistic based on the original data.

The second topic of discussion in this tutorial will be an introduction to extreme value statistics. Extreme values statistics have proven useful in ocean engineering (e.g. highest wave height), meteorology (highest amount of rainfall, maximum wind speed), and in investigating fatigue strength and corrosion. Here the focus is on the extremes of a measured parameter instead of the typical focus on centralized tendencies such as the mean or median. I believe that they could also prove useful in exploring electrical reliability issues such as the highest (lowest) use temperature for a metal line, maximum use current flow through a specific device, or the highest use voltage across a capacitor.

Flash Memory Reliability

Alberto Modelli and Angelo Visconti, ST Microelectronics

Tutorial C1, Monday, 4:00-5:00 p.m. (Angora Room)

Memory reliability is a key issue of flash technology. The continuous trend to increase the storage density is driving the technology close to its physical limits and new reliability challenges are met. The tutorial will discuss the failure mechanisms limiting memory endurance and data retention. Reference will be done to the two mainstream flash technologies, considering a floating-gate cell in a NOR- or NAND-type memory array. The first part of the tutorial is dedicated to failure modes related to the intrinsic cell behavior. Classical data loss mechanisms and the degradation of the oxide properties caused by high-field tunneling or channel hot electron injection will be examined. The second part deals with single-cell failures, in particular low-temperature data loss after program/erase cycling, which can be ascribed to tunnel oxide defects. The nature of the leakage current and its relation to the Stress-Induced Leakage Current observed in large area capacitors will be discussed. Design solutions to solve or, at least, ease this issue will be considered.

Radiation Hardened CMOS at Commercial Foundries: Radiation Environments & Techniques to Mitigate Radiation Effects

Ron Lacoe, Aerospace Corp.

Tutorial D1, Monday, 4:00-5:00 p.m. (Cathedral Room)

Recently, a novel approach for fabricating radiation-hardened components at commercial CMOS foundries (as opposed to specialized foundries) has been developed. In this approach, radiation hardness is designed into the component using non-standard transistor topologies, the addition of guard rings and the application of novel circuit techniques. This presentation will begin with a description of the space and terrestrial radiation environments, followed by a discussion on the effects of different radiation sources on CMOS technologies. This will include a discussion on total-ionizing dose, single-event upsets, single-event latchup and single-event transient radiation effects. Specific non-standard transistor topologies and the application of guard bands to mitigate total dose effects will be discussed. Circuit approaches to mitigating single-event effects will also be presented. The application of these design approaches does not come without area and performance penalties, which will be quantified as part of this presentation.

Design-in Reliability with Emphasis on NBTI

Chittoor Parthasarathy, ST Alliance

Tutorial C2, Monday, 5:00-6:00 p.m. (Angora Room)

The advent of NBTI (Negative Bias Temperature Instability) as a prominent degradation mechanism and a host of other factors - diverse offerings from a

(continued on back of registration form)

2005 IEEE INTERNATIONAL
INTEGRATED RELIABILITY WORKSHOP
PROGRAM

MONDAY, October 17

Please have lunch before arriving at the camp; no lunch will be served at the camp.

1:00 – 6:00 p.m. Registration (*Lodge Lounge*): Pick up badges & handout; sign up for discussion groups and SIG's; prepare posters

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key, with lodge area map and information. (If physically challenged please notify desk of special needs.)

1:30 – 3:30 p.m. **Tutorials** (parallel sessions A & B, see abstracts)

	Angora Rm.	Cathedral Rm.
1:30–2:30	A1: Dielectrics	B1: MEMS
2:30–3:30	A2: High-K Defects	B2: Statistics

3:30 – 4:00 p.m. Break (poster preparation)

4:00 – 6:00 p.m. **Tutorials** (parallel sessions C & D, see abstracts)

	Angora Rm.	Cathedral Rm.
4:00–5:00	C1: Flash Memory	D1: Radiation
5:00–6:00	C2: NBTI	D2: Product

6:15 – 7:30 p.m. DINNER, *(Dining Room)* authors: dine with your session chair

7:30 – 7:40 p.m. Announcements, DGs, SIGs *(Cathedral Room)*

7:40 –10:00 p.m. Poster Session & Mixer *(Cathedral Room)*

TUESDAY, October 18

7:00 – 8:00 a.m. BREAKFAST *(Dining Room)*

8:15 – 8:30 a.m. Welcome & Introduction: Rolf Vollertsen, General Chair
Technical Program Overview: John Conley, Tech. Prog. Chair *(Angora Room)*

8:30 – 9:30 a.m. Keynote: Status and Future Trends in Technology Reliability: Balancing Technical Challenges and Affordability—Dr. Erwin Hammerl, Director of Reliability Methodology, Infineon Technologies

9:30 – 9:50 a.m. Break

9:50 –11:30 a.m. **SESSION #1: NBTI,** Chairs: John Conley, Sharp Labs and Guillaume Ribes, STMicroelectronics / IMEP/ENSERG

- 1.1 Observations of NBTI-induced atomic scale defects—J.P. Campbell, P.M. Lenahan, Penn State Univ, A.T. Krishnan, S. Krishnan, Texas Instr.
- 1.2 Single-hole detrapping events in pMOSFETs NBTI degradation—V. Huard, Philips Semiconductors, M. Denais, C.R. Parthasarathy, STMicroelectronics
- 1.3 Combined effect of NBTI and channel hot carrier effects in pMOSFETs—C. Guerin[1], V. Huard[2], M. Denais[1], F. Perrier[2], [1]STMicroelectronics., [2]Philips Semiconductors
- 1.4 NBTI in SOI PMOSFETs with nitrogen in the gate oxide—S.T. Liu[1], D.E. Ioannou[2], D.P. Ioannou[2], M. Flanery[1], H.L. Hughes[3] [1]Honeywell Defense & Space Elect. Syst., [2]George Mason Univ., [3]Naval Research Laboratory

11:30 – 12:00 p.m. Group Picture

12:00 – 1:00 p.m. LUNCH, *Dining Room*

1:00 – 3:05 p.m **SESSION #2: Cu / LOW-k I**, Chairs: Harry Schafft, NIST and Peter O'Shea, PMC Sierra

- T.E TUTORIAL E: Back-end reliability—Glenn Alers, Novellus
- 2.1 Via depletion electromigration in copper interconnects—C. Christiansen, B. Li, J. Gill, R. Filippi, M. Angyal, IBM
- 2.2 Blech effect in dual damascene copper-low k interconnects—D. Ney[1,3], X. Federspiel[2], V. Girault[1], O. Thomas[3], P. Gergaud[3], [1]STMicroelectronics, [2]Philips Semiconductors, [3]TECSEN

3:05 – 3:25 p.m. Break

3:25 – 5:05 p.m. **SESSION #3: Cu / LOW-k II**, Chairs: Glenn Alers, Novellus and Tim Sullivan, IBM

- 3.1 Resistivity of nanometer-scale film and line interconnects: model, simulation, measurement—A.E. Yarimbiyik[1,2], H.A. Schafft[2], R.A. Allen[2], M.E Zaghloul[1], D.L. Blackburn[2] [1]George Washington Univ., [2]NIST
- 3.2 An integrated solution with a novel bi-layer etch stop to eliminate 90 nm Cu/low k package fail—P. Sun, E. Bei, Y.W. Chen, T. Hu, F. Ji, C.C. Liao, V. Ruan, A. Tsai, D.L. Wang, S. Wu, G. Zhang, A. Fan, I.C. Chen, SMIC
- 3.3 Impact of moisture on porous low-k reliability—J. Michelon, R.J.O.M. Hoofman, Philips Research Leuven
- 3.4 Effect of moisture on the Time Dependent Dielectric Breakdown (TDDB) behavior of and ultra-low-k (ULK) dielectric—J.R. Lloyd, T.M. Shaw, E. Liniger, IBM Thomas J. Watson Research Center

5:05 – 6:00 p.m. Mixer & Poster Session

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 9:00 p.m. Discussion Groups, Chair: *Yvonne Nelson, Qualcomm*

90 min parallel sessions, attendees are to participate in one of the groups:

1. NBTI
2. Interconnect
3. Gate Oxide / High-k
4. Product/Circuit

9:00 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

WEDNESDAY, October 19

7:00 – 8:00 a.m. BREAKFAST *(Dinning Room)*

8:00 – 8:15 a.m. Announcements, *(Angora Room)*

8:15 – 10:10 a.m. **SESSION #4: DIELECTRICS AND HOT CARRIERS**, Chairs: Bill Knowlton, Boise State Univ. and John Suehle, NIST

- 4.1 Voltage acceleration of oxide breakdown in the sub-10nm Fowler-Nordheim and direct tunneling regime—R. Duschl, R.P. Vollertsen, Infineon Technologies
- 4.2 Design for ASIC reliability for low temperature applications—Y. Chen, M. Mojaradi, L. Westergard[1], C. Billman[1], S. Cozy, G. Burke, E. Kolawa, JPL [1]AMI Semiconductors
- 4.3 Lifetime prediction of ultra-thin gate oxide PMOSFETs submitted to hot hole injection—T. Di Gilio, A. Bravaix, L2MP/ISEN
- 4.4 A new degradation mode for advanced heterojunction bipolar transistors under reverse bias stress—M. Ruat, R. Angers, N. Revil, STMicroelectronics, G. Ghibaudo, G. Pananakakis, IMEP/ENSERG

10:10 – 10:30 a.m. Break

10:30 – 11:45 a.m. **SESSION #5: CIRCUITS AND MEMORY**, Chairs: Bill Tonti, IBM and Yuan Chen, Jet Propulsion Lab

- 5.1 Degradation of rise time in NAND gates using 2.0 nm gate dielectrics—M.L. Ogas, P.M. Price, J.C. Kiepert, R.J. Baker, G. Bersuker[1], W.B. Knowlton, Boise State Univ. [1]SEMATECH
- 5.2 Charge retention of silicided and unsilicide floating gates embedded logic nonvolatile memory—B. Wang, H. Nguyen, Impinj
- 5.3 On intrinsic failure rate of products with error correction—G. Tao, J. Bisschop, S. Nath, Philips Semiconductors

12:00 – 1:30 p.m. LUNCH (*Dining Room* — Take out Lunch bags available)

1:30 – 5:00 p.m. Open The afternoon is free for discussion, hiking & other recreation

5:00 – 6:00 p.m. Mixer & Poster Session

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 9:00 p.m. Discussion Groups, Chair: *Yvonne Nelson, Qualcomm*

90 min parallel sessions, attendees are to participate in one of the groups:

1. NBTI
2. Interconnect
3. Gate Oxide / High-k
4. Product/Circuit

9:00 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

THURSDAY, October 20

7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)

8:15 – 8:30 a.m. Announcements, *(Angora Room)*

8:30 – 10:35 a.m. **SESSION #6: HIGH-k DIELECTRICS**, Chairs: Pat Lenahan, Penn State Univ. and Robin Degraeve, IMEC

- 6.1 Asymmetries in the electrical activity of intrinsic grain-boundary and O-atom vacancy defects in HfO_2/ZrO_2, and at their interfaces with SiO_2: a disabling flaw for CMOS gate dielectric applications—G. Lucovsky, C. Fluton, C. Hinkle, S. Lee, North Carolina State Univ., J. Lüning, Stanford Synchrotron Research Center
- 6.2 Physical origin of V_t instabilities in high-k dielectrics and process optimisation—G. Ribes[1,2], S. Bruyère[1], D. Roy[1], C. Parthasarthy[1], M. Müller[4], M. Denais[1,3], V. Huard[4], T. Skotnicki[1], G. Ghibaudo[2] [1]STMicroelectronics, [2]IMEP/ENSERG, [3]L2MP/ISEM, [4]Philips
- 6.3 Detection of trap generation in kigh-k gate stacks—C.D. Young, D. Heh[1], S. Nadkarni, R. Choi, J.J. Peterson, H.R. Harris, J.H. Sim, S.A. Krishnan, H. Barnett, E. Vogel[1], B.H. Lee, P. Zeitzoff, G.A. Brown, G. Bersuker, SEMATECH [1]NIST
- 6.4 Charge instability in high-k gate stacks with metal and polysilicon electrodes—A. Neugroschel, Univ. of Florida, G. Bersuker, SEMATECH
- 6.5 Charge trapping dependence on the physical structure of ultra-thin ALD-HfSiON/TiN gate stacks—S.A. Krishnan, M.A. Quevedo-Lopez, R. Choi, P.D. Kirsch, C. Young, R. Harris, J.J. Peterson, H. Li, B.H. Lee, SEMATECH, J.C. Lee, Univ. of Texas at Austin

10:35 – 11:00 a.m. Break (If you haven't already done so, please check out!)

11:00 – 12:00 p.m. DG Summary / SIG Report / Wrap-up

Noon – 1:20 p.m. LUNCH, *(Dining Room)* & then the Workshop Ends—Attendees must Leave the Stanford Sierra Camp unless attending JC14.2

2:00 p.m. JEDEC 14.2 Committee on Wafer Level Reliability Meeting

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2005 IIRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 20-21)

Meeting registration automatically includes a room reservation.

(Please type, print or attach business card)

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Last First Initial

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Email: ____________________________

For cabin assignments: ❑ male ❑ female

❑ Address is HOME

❑ Please check here if you do not wish to receive mail other than from IIRW & IRPS

❑ Please check here if physically challenged and you require any auxiliary aids or services. Please call (315) 339-3968.

❑ Will bring poster. Title: ____________________________

I am interested in the following Discussion Group(s):

❑ High-k; ❑ NBTI; ❑ Interconnects; ❑ Oxide; ❑ Product Reliability;

❑ My Suggestion ____________________________

Method of Payment: ❑Check: Make checks payable to: **2005 IEEE/IIRW**

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ADVANCE REGISTRATION FEES

IEEE Member (incl. mem#__________) **$1045*** ________

NON-IEEE Member .... **$1145*** ________

IEEE STUDENT** (mem#__________) **$750*** ________

After 7-Oct-05 add late fee $100 ________

** Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday— lunch Thursday), Final Workshop Report with CD.*

***To promote student involvement at IIRW, we will be offering a reduced registration fee of $750 to the **first 15 students** who register . Students accepting the discount must be either IEEE member, or join the IEEE as a student member.*

EXTRA COPIES of Workshop?

Final Report (printed) Qty:__ x **$80** ________

Final Report (CD) .... Qty.___x **$80** ________

Final Report (printed & CD) Qty:__ x**$130** ________

JC-14.2 Mtg. accommodations*** **$250** ________

**** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)*

TOTAL REMITTED $ ____________

No wire transfers Cancellation fees: $50 after Sept. 23 ; full fee after Oct. 7

Send this completed form and payment to: IIRW Registration; P.O. Box 308; Westmoreland, NY 13490 Paying by credit card... fax to 315-336-9134
Questions? becky@sar101.com or 315-339-3968 or web site: http://www.iirw.org

(cont. from page 2)
technology node, complex products and aggressive performance targets - are prompting efforts to develop methodology to analyze device degradation at circuit/design level with a view to preempt problems later on. The aim of this tutorial is to elaborate this "Design-in Reliability" (DiR) methodology applied to CMOS circuits. In the past, DiR has mainly addressed degradation due to hot-carrier injection (HCI). In this tutorial, we shall focus on tackling NBTI degradation, individually as well as in conjunction with HCI.

We shall begin by reviewing recent developments in understanding NBTI and HCI phenomena and shall discuss implementations of degradation models for SPICE. Subsequently, we shall look into the aspect of reliability simulation - methods of degradation analysis applied during circuit simulation. In the final section, we shall address the aspect of reliability analysis for different classes of designs from a designer viewpoint: (a) role of operating conditions, modes and stimuli, (b) minimizing the effects of degradation and (c) correlation of predicted results with silicon. The tone in general shall be to highlight open issues and explore their solutions. We shall conclude by pondering on how the DiR methodology is set to evolve in the future.

A Survey of Product Reliability in 90nm CMOS and Beyond

Andrew Turner, IBM

Tutorial D2, Monday, 5:00-6:00 p.m. (Cathedral Room)

While 90 nm and 45 nm CMOS matures from the lab to the manufacturing floor, the reliability of the product becomes more important as defect densities and degradation mechanisms that affect microprocessors may not be observable in sufficient quantities or magnitude at the macro level. There is a need to understand that the interaction between design and manufacturing, as it relates to field reliability, is moving beyond test-site measurements and design simulation alone. Understanding the product reliability and performance metrics through the useful life of the product is imperative. This often requires knowledge of the most sensitive circuits and the mechanisms that are most likely to negatively affect them. Tracking these metrics through an accelerated life stress and evaluating fails is the best bet for successful product qualification.

Back End Reliability—*Glenn Alers, Novellus Systems*

Tutorial E, Tuesday, 1:00-2:00 p.m. (Angora Room)

As interconnects become responsible for a larger portion of signal delays in advanced circuits the pressure for aggressive scaling will increase. Current densities will increase as dimensions are reduced and stress management will be more critical as the compliance of low-k materials decreases. However, reducing the interconnect dimensions tend to degrade reliability as the critical volume associated with a failure decreases. This talk will review the conflicting requirements for reliability and product performance and the solutions that are being pursued. Several paths are available for improving electromigration including advanced barriers, copper alloy seed layers and metallic cap layers. However, each of these solutions will come at the cost of line resistance, which is already increasing due to increased scattering in small geometries. Stress migration will become a larger concern at small dimensions because both the absolute stress level and stress gradients will increase at smaller geometries. Reducing the density of the inter-level dielectric will exaggerate these problems due to intrinsically lower adhesion energies and an increased diffusivity of copper, water and ammines in the dielectric. Ultimately, it will be reliability that limits the scaling of interconnects for future nodes.

DISCUSSION GROUPS–Chair: Yvonne Nelson, Qualcomm

Attendees will have a choice of four areas on Tuesday and Wednesday evenings. The specific topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of moderators who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. Please see http://www.iirw.org/05/DG.html for up to date details. This year's discussion areas and moderators are:

1. *Interconnect reliability:*
   John Euler (Qualitau) & Tim Sullivan (IBM Microelectronics)
2. *NBTI:*
   Jason Campbell (Penn St. Univ.) & Vincent Huard (Philips Semi.)
3. *Gate oxide / High-k reliability:*
   Guillaume Ribes (STM) and John Suehle (NIST)
4. *Product/Circuit reliability:*
   Mark Porter (Medtronic) and t.b.a.

SPECIAL INTEREST GROUPS

Chair: Yvonne Nelson, Qualcomm

The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. For the latest information on SIGs, please see http://www.iirw.org/sig/2005SIG.html.

REFEREED & OPEN POSTER SESSIONS

(Monday, Tuesday, and Wednesday Evenings)

Chair: Patrick Lenahan, Penn State University

In addition to our refereed poster sessions featured below, all attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate in the space provided on the registration form your intention to bring a poster. A poster display board (32" x 40" or 81 cm x 100 cm) will be reserved for you. Your work should be in landscape format on 8½ x 11" or A4 paper with a maximum of twelve pages. In addition, all open poster presenters are invited to submit a two-page abstract of your presentation for inclusion in the Workshop Final Report. See http://www.iirw.org/05/Poster.html for details and deadlines. Also feel free to bring last minute results, board space will be found for you.

IIRW 2005 Refereed Posters:

P1 Testing methodology for lifetime extrapolation of pzt capacitors—E. Bouyssou[1,2], S. Bruyère[2], G. Guégan[2], C. Anceau[2], A. Agostini[1,2], R. Jérisian[1] [1]Université de Tours—LMP; [2]STMicroelectronics

P2 Efficient fWLR inline monitoring of hot carrier reliability by means of one simple, comprehensive parameter—R. Vollertsen, H. Nielen, Infineon Technologies

P3 An investigation on stacked NMOSFET with different poly-gates bias conditions under ESD stress in 0.13µm CMOS tolerant I/O circuit—C.-Y. Huang, G. Chen, United Microelectronics Corp.

P4 Impact of NBTI-driven parameter degradation on lifetime of a 90nm p-MOSFET—R. Wittmann[1], H. Puchner[2], L. Hinh[2], H. Ceric[1], A. Gehring[3], S. Selberherr[1] [1]Technical University at Wien; [2]Cypress Semiconductor; [3]AMD Saxony

P5 Hot carrier effect on CMOS class e power amplifiers—E. Xiao, UT Arlington

P6 The novel mechanism of temperature effect in ultra-thin oxide breakdown—J. Shieh, T.-K. Kang, C.-L. Lin, O. Lo, J.-P. Chen, K.C. Su, UMC

P7 Impact of device scaling on deep sub-micron transistor reliability - A study of reliability trends using SRAM—M. White[1,2], Z. Gur[2], M. Talmor[2], B. Huang[2], J. Qin[2], X. Li[2], X. Zhang[2], Y. Chen[1], D. Nguyen[1], J. Bernstein[2] [1]JPL; [2]University of Maryland

P8 Matching variation after HCI stress in advanced CMOS technology for analog applications—J. C. Lin[1,3], S.Y. Chen[2], H.W. Chen[2], H.C. Lin[2], Z.W. Jhou[2], S. Chou[1], J. Ko[1], T.F. Lei[3], H.S. Haung[2] [1]United Microelectronics Corp.; [2]National Taipei University of Technology; [3]National Chiao Tung University

P9 One time programming device yield study based on anti-fuse gate oxide breakdown on P-type and N-type substrates—N. Mathur, Y. Ahn, I. Kouznetov, F. Jenne, J. Fulford, Cypress Semiconductor Inc.

P10 Length scaling effects on dual damascene copper interconnects electromigration—M.H. Lin, K.P. Chang, K.C. Su, UMC, T. Wang, National Chiao-Tung Univ.

P11 IREM usage in the detection of highly resistive failures on 65 nm products—I. Wan, D. Bockelman, Y. Xuan, S. Chen, Intel

P12 Predictive simulation to improve reliability of a snapback-based NMOS clamp—P. Gaitonde et al., Florida Institute of Technology

P13 An investigation on substrate current and hot carrier degradation at elevated temperatures for nMOSFETs of 0.13 µm technology—J. C. Lin et al., UMC

P14 Determination and characterization of EOS-induced on submicron devices using 2D IR spectral imaging technique—M.F. Bailon, P.F.F. Salinas, J.P.S. Arboleda, J.J.C. Miranda, Intel Tech. Philippines

P15 First steps toward aging simulation of complex analog circuits with behavioural modeling—F. Marc, Y. Danto, Université Bordeaux

P16 Some applications of V_{bd} and Q_{bd} tests—J.T.C. Chen, T. Dimitrova, D. Dimitrov, Four Dimensions, D.K. Schroder, Arizona State University

JEDEC 14.2 Wafer Level Reliability Standards Meeting—will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $250.00, which includes Thursday night dinner and lodging, and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558, see www.jedec.org, or contact Al Strong (astrong@us.ibm.com), JC-14.2 Chair, at (802) 769-1326.

More Detailed Information. Web site: www.iirw.org. If you have additional questions, please contact me, the Technical Program Chair, John Conley or other committee contacts identified on the front of this announcement. We look forward to seeing you at the Workshop!

Sincerely,

John F. Conley, Jr.

John F. Conley, Jr.
Technical Program Chair

IIRW TRAVEL ARRANGEMENTS AND ACCOMMODATIONS

ARRIVAL AT CONFERENCE CENTER (a.k.a. CAMP)

For those who are planning to attend the first tutorials, please plan to arrive *after* you have had your lunch. The Conference Center will **not** be prepared to serve you lunch. We will be ready to register you by 1:00 p.m. If you are coming later, we recommend you arrive before dark because the road from Route 89 is mostly one lane and winding.

TRANSPORTATION

The Stanford Sierra Conference Center is located at the far end of Fallen Leaf Lake, several miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Flight arrangements into Reno can be made through the *IEEE Travel Services*. Driving time from the Reno airport to the Stanford Sierra Conference Center is approximately two hours. Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***South Tahoe Express.*** With a scheduled request, Stanford Sierra Conference Center will provide transportation from the Casino to the Conference Center.

TRAVEL ARRANGEMENTS AND DISCOUNTS

Special discounted airfares for IIRW are available through IEEE Travel Services. Discounts are available with American, Continental and United Airlines. If you are flying on another carrier, contact IEEE Global Travel Services to check for other discounts by calling 1-800-879-4333 (US and Canada) and 1- 732-562-5387 (International) between the hours of 8:30 a.m. and 5:00 p.m. EST, Monday through Friday, or check http://www.ieeetravelonline.org and click on "Book a Flight." This secure site offers simple and convenient service through which you can search, reserve and ticket your travel anytime, anywhere. Discounts are only available through IEEE Travel Services for air.

Special car rental rates are available with the following companies:

National Car Rental .... Discount Code: 5282921
Avis Rental Car .... Discount Code: A606098
Budget Rental .... Discount Code: X520000
Hertz Rental .... Corporate Code: 61368,
Permission Code: 937661
Enterprise Rental .... Corporate CDP# NA24IE1

You may also fax or email your travel requirements including your travel dates, preferred departure and return times, and phone and fax numbers to the IEEE Travel Services; and a Travel Counselor will contact you promptly. Fax: +1 732 562 8815 ; e-mail address: travel-team@ieee.org

IEEE Travel goes the extra miles for its customers - more than today's no-service internet travel sites. Customers receive extra benefits like: dedicated, experienced travel counselors, 24-hour emergency service, automated fare quotes, and much more!

TRAVEL between RENO and SOUTH LAKE TAHOE

The South Tahoe Express **runs a shuttle from Reno to South Lake Tahoe** with departures from Reno on the hour from 10:00 a.m, to 7:00 p.m. and and the travel time is approximately 1½ hours. The shuttle costs $21 each way ($38 round trip) tickets can be purchased at the South Tahoe Express counter located in the baggage area in the Reno airport. Check http://www.southtahoeexpress.com/ to access the self serve ticketing system and verify schedules that are seasonal and subject to change or call 866-89-TAHOE or +1775 325-8944).

The South Tahoe Express shuttle **leaves the Horizon Casino at South Lake Tahoe and returns to Reno** on the following schedule: 3:37 a.m., 5:07, 7:37, 8:37, 10:37, 12:37, 1:37 p.m., 2:37, 3:37, 5:37, and 8:52 p.m. Tickets may be purchased at the main cashier's cage in the Horizon Casino.

TRAVEL between SOUTH LAKE TAHOE and STANFORD SIERRA CONFERENCE CENTER

Stanford Sierra Conference Center offers courtesy transportation for conference attendees from the Horizon Casino between 12:30 p.m. and 11 p.m. on Registration Day (Monday, Oct. 17). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the South Tahoe Express, please notify Stanford Sierra Conference Center (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the Conference Center at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino. for more information, visit http://www.stanfordalumni.org/learningtravel/sierra/sierra-center/shuttle.html.

ACCOMMODATIONS

The Stanford Sierra Conference Center provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note that while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks. Please be aware of the following items:

- All participants must stay at the camp during the workshop.
- We cannot accommodate spouses or any companions at the camp.
- Accommodations are not available at the Stanford Conference Center for any day before or after the workshop.
- Smoking is permitted outdoors only. Smoking is not permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls: (530) 541-1244.
- There are pay telephones for outgoing calls and there are no telephones in the rooms.
- Please have lunch before you arrive at the Conference Center, there is no lunch available on Monday.

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IRW!

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the Conference Center. A small flashlight would be helpful to find your cabin after dark.

See http://www.iirw.org/Directions_from_Reno_Airport.htm for detailed driving directions from the Reno Airport to Conference Center.