



2003 *International* INTEGRATED RELIABILITY WORKSHOP



October 20-23, 2003

<http://www.irps.org/irw/>

Stanford Sierra Camp, Lake Tahoe, CA

CALL FOR PAPERS

The Integrated Reliability Workshop continues to focus on ensuring semiconductor reliability through component fabrication, design, characterization, and analysis tools. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications.

Hot reliability topics of the workshop are: high-k gate dielectrics, Cu-interconnects & Low-k dielectrics, reliability of deep sub-micron, high speed, high frequency devices (e.g. SiGe), SOI devices, reliability modeling & simulation, and the reliability of future technologies such as molecular electronics and carbon nanotubes.

We invite you to submit a presentation proposal that addresses one or more of the following topics:

• **WAFER LEVEL RELIABILITY TESTS AND TEST APPROACHES:**

fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data; success stories; the fine tuning of a WLR implementation; accounting for censoring

• **IDENTIFICATION OF NEW RELIABILITY EFFECTS & CHARACTERIZATION:**

failure mechanisms in new materials and devices; reliability aspects of: high-k gate stack, Cu-interconnects & low-k dielectrics, MOS and bipolar transistors, MEMS devices, MRAM, molecular transistors, carbon nanotubes, etc.; device/structure reliability concerns; and limits to accelerated stress.

• **RELIABILITY MODELS AND SIMULATIONS:**

nature of defects; physical and electrical characterization of defects; defect generation models; modeling of dielectric structures and properties; and modeling/simulation of reliability related circuit constraints

• **RELIABILITY TEST STRUCTURES:**

design, characterization, and data analysis for chip or package level circuit-like structures (including electrical and/or physical test/analysis).

• **CUSTOMER PRODUCT RELIABILITY REQUIREMENTS/
MANUFACTURER RELIABILITY TASKS:**

limits to achieve future reliability targets, reliability evaluation methodologies; reporting systems; data base, wafer and package burn-in and strategies to eliminate burn-in.

• **DESIGNING-IN RELIABILITY**

(CIRCUITS, PROCESSES, PRODUCTS):

methodologies and concepts, modeling, simulation tools, reliability-driven design rules and checkers; use of WLR for design rule verification.

SUBMISSION DEADLINE: *Received by July 6, 2003.*

Your submission should state clearly and concisely the results of your work and why they are significant. Representative data and/or figures that support your proposal are REQUIRED. This year we are accepting both paper and poster submissions. Please state which submission category you prefer.

Please e-mail your maximum two-page abstract (incl. figures). Send it as a MS Word document or pdf file. Your proposal must include the name, affiliation, complete return address, telephone and telefax numbers, and e-mail address for each author. Telefax submissions will NOT be accepted. All submissions will be acknowledged within three weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair.

MAIL TO: Al Strong, Technical Program Chair, astrong@us.ibm.com
IBM Microelectronics, mail #967A
1000 River Road
Essex Junction, VT 05452

Visual aids for the ACCEPTED paper proposals are required by September 16, 2003 for inclusion in the Presentation Handout available at the workshop. A written version of your presentation is due at the workshop for inclusion in the Final Report.

LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin cluster is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Lodging is available for meeting attendees only.

HISTORY

The Wafer Level Reliability Workshop was initiated in 1982 through the efforts of O. D. "Bud" Trapp, of Technology Associates, and the active support and encouragement of DARPA (Defense Advanced Research Projects Agency). This support continued for the first eight years of the Workshop and included active support and involvement of the Stanford University Integrated Circuits Laboratory and the University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences. After DARPA sponsorship ended, Bud Trapp continued the direction of the Workshop until 1991 after which time he requested that sponsorship and management be assumed by an appropriate professional association. The IEEE accepted this responsibility in 1992. In 1993, the name of the Workshop was changed to the Integrated Reliability Workshop. This change reflects the enlarged scope of the Workshop, the integrated nature of reliability in the manufacture of semiconductor products, and the need for a broader and a more comprehensive approach to reliability engineering.

SPONSORS

The International Integrated Reliability Workshop is sponsored and managed by the IEEE Electron Device Society and the IEEE Reliability Society through the Board of Directors of the International Reliability Physics Symposium.

