



IEEE
2003 International
INTTEGRATED
RELIABILITY
WORKSHOP

Stanford Sierra Camp, S. Lake Tahoe, CA
October 20-23, 2003 <http://www.irps.org/irw/>

IEEE/Integrated Reliability Workshop
P.O. Box 308
Westmoreland, NY 13490-0308

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Linda M. Head, Rowan Univ.

You are cordially invited to participate in the 2003 Integrated Reliability Workshop. It provides a unique environment for envisioning, discussing, and developing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning.

MAJOR TECHNICAL THEMES

As industry retools and regroups for the coming technology sector expansion, it is crucial that the reliability of new materials, devices, and products be kept at the forefront of development and design of new products. The Integrated Reliability Workshop is focused this year on exactly this mission.

On Monday, we are leading our program this year with tutorials on three diverse but important topics in materials and product reliability, "Theory and Application of Non-Contact Methods for In-Line Reliability Determination," by John D'Amico, Semiconductor Diagnostics, Inc., "Fast Wafer Level Reliability Monitoring of Product Wafers" by Andreas Martin, Infineon Technologies, and "MRAM and Reliability" by Brian Hughes, Infineon Technologies.

An additional tutorial session on Tuesday includes a late-breaking news presentation "Reliability Physics and Chemistry of Thin and High-k Gate Oxides" by Pat Lenahan, Penn State, which addresses new materials reliability issues in detail.

Our keynote picks up on another important theme, metrology and physical characterization for new technologies. It is "The Complete Metrology Roadmap" by Alain C. Diebold, International SEMATECH Senior Fellow.

You will have ample time for one-on-one exchange, organized discussion groups, our popular and productive SIGs (Special Interest Groups) and poster sessions where all our attendees are encouraged to display a poster with their most recent work, ideas, and results. As a very special feature, you are offered the opportunity to view three recent IEEE sponsored videos: "Oxide Wearout/Breakdown/Reliability," "MEMS Performance & Reliability," and "Accelerated Stress Testing." To purchase these videos for your organization is costly but IRW attendees can view them free of charge at the Workshop.

Inform your colleagues about the workshop and spread the word, so nobody misses the chance to participate and benefit. Inform your management. Your organization will not want to miss this investment in education on how to deal with today's reliability issues and prepare for the ones of tomorrow.

'03 Workshop Features:

- ★ **Keynote: "The Complete Metrology Roadmap," Alain C. Diebold, International SEMATECH, USA**
- ★ **Group Discussions**
 - WLR and EM
 - Ultra-thin and high-k dielectrics
- ★ **Tutorials**
 - Reliability Physics and Chemistry of Thin and High-k Gate
 - Fast Wafer Level Reliability Monitoring of Product Wafers
 - Non-Contact Methods for In-Line Reliability Determination
 - MRAM and Reliability
- ★ **19 Technical Presentations on:**
 - Customer Product Reliability Requirements
 - Ultra-Thin Oxides & High-K Dielectrics
 - Circuit Level Reliability
 - Hot Carriers and Memory Reliability
- ★ **Three Videos on:**
 - Oxide Wearout/Breakdown/Reliability
 - MEMS Performance & Reliability
 - Accelerated Stress Testing
- ★ **Refereed/Open Poster Sessions**
- ★ **Special Interest Groups**



KEYNOTE

THE COMPLETE METROLOGY ROADMAP

Alain C. Diebold, International SEMATECH, USA

The Metrology Roadmap is now a well established part of the International Technology Roadmap for Semiconductors. The Metrology Roadmap describes the measurement requirements and potential solutions for lithography, front end processes, and interconnect processes. The Metrology Roadmap hopes to link together measurement needs and process requirements. One well known example of this connection is to calculate the precision required for measuring the thickness of a gate dielectric when the allowed process range is 4% to 3σ . The precision requirements for many measurements are notoriously difficult to meet. Based on the precision requirements for future technology generations, critical dimension control will be difficult to maintain using known measurement methods (CD-SEM, scatterometry, etc.). An extended discussion of the Metrology Roadmap including Materials Characterization will be provided

TUTORIALS

Chair: Amr Haggag, Motorola

Tutorial #1 Monday, 1:30–3:30 p.m. (Angora Room)

THEORY AND APPLICATION OF NON-CONTACT METHODS FOR IN-LINE RELIABILITY DETERMINATION

John D'Amico, Semiconductor Diagnostics, Inc.

Over the last decade, the IC industry has labored vigorously to maintain Moore's law. Success, in large part, has been due to realizing critical milestones – such as transitioning to larger diameter wafers, integrating Cu and Low K interconnects, and pushing the physical boundaries of the gate oxide – not to mention overcoming the countless other processing and integration challenges encountered. During the same time, the cost invested per wafer, as measured by the number and complexity of the processes, has grown significantly. Naturally, to protect the investment and maximize efficiency, there is gravitation toward in-line, real-time reliability monitoring to identify and diagnose issues before they kill yield.

In this regard, in-line monitoring of the front-end diffusion area has become increasingly more common and mature. Numerous non-contact measurements are now available that provide fast feedback of parameters ranging from silicon lifetime to gate oxide integrity. This tutorial provides an in-depth examination of the theory and application of in-line characterization methods developed from two fundamental non-contact measurement techniques, Surface Photovoltage (SPV) and Contact Potential Difference (CPD), and their response to stress created by dielectric charging with a corona discharge in air. Specific topics include monitoring of heavy metal contamination, mobile ion contamination, leakage current, and interface and dielectric traps, with an emphasis placed on reliability issues for ultra-thin gate dielectrics.

Tutorial #2, Monday, 4:00–6:00 p.m. (Angora Room)

FAST WAFER LEVEL RELIABILITY MONITORING OF PRODUCT WAFERS

Andreas Martin, Infineon Technologies

This tutorial gives an overview of the current state of the art of fast Wafer Level Reliability (WLR) monitoring. Fast WLR is an

essential tool for a continuous quality control in a production environment to verify the process reliability beyond process qualification on product wafer material. This in-line testing method, taking a few seconds per test item, guarantees shortest feedback cycles into production to detect process reliability deviations. Of course, it can be also employed before process qualification, during process development.

This tutorial describes the main aspects and highlights problem areas of: test structure design for scribe lines, stress and measurement sequence creation, tester hardware, analysis/reporting and sampling. It discusses the controversy between qualitative and predictive fast WLR, how to use fast WLR even without a physical model for the degradation mechanism. The typical areas of dielectric reliability (MOS gate dielectrics, back end of line capacitors, intermetal dielectrics), device degradation (Hot Carrier, negative bias temperature instability, mobile ions), metallisation reliability (electromigration, contact and via integrity) and effects of plasma induced damage are covered. Relevant publications of the field are stated for further studies.

Tutorial #3, Monday, 7:30–8:30 p.m. (Angora Room)

MRAM AND RELIABILITY

Brian Hughes, Infineon Technologies

This tutorial will provide an overview of the design, operation, and materials of Magnetoresistive Random Access Memory (MRAM) with emphasis from a reliability engineering perspective. The speaker will provide background information on MRAM architectures and discuss novel reliability problems inherent to MRAM. Reliability issues and concerns will be discussed and illustrated with examples wherever possible. The intention of the tutorial is to give attendees a basic and broad introduction to the reliability challenges raised by this novel memory form.

Tutorial #4, Tues., 1:00–3:00 p.m. (Cathedral Room)

RELIABILITY PHYSICS AND CHEMISTRY OF THIN AND HIGH-K GATE OXIDES

Pat Lenahan, Pennsylvania State University

The International Technology Roadmap for Semiconductors indicates that fundamental limits to downscaling will be reached by 2005. At the present time, there is therefore great technological interest in very thin SiO₂-based dielectrics as well as in "new" significantly higher dielectric constant (high-k) materials such as HfO₂, ZrO₂, and hafnium and zirconium silicates. These new oxides have considerable promise but many recent studies demonstrate that devices based upon these and other high-k oxides exhibit potentially serious reliability problems which are as yet poorly understood. This tutorial will review recent work of a number of groups investigating dielectric charge trapping, interface traps, low channel mobilities, and other problems in new high-k oxide/silicon systems. This review will be integrated with a discussion of somewhat better understood problems in very thin SiO₂-based dielectric/silicon systems. This presentation will also include a comparison of atomic scale defects involved in hafnium oxide – hafnium silicate, zirconium oxide – zirconium silicate, and silicon dioxide based systems.

(continued on back of registration form)



2003 *International*

INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 20

- 1:00 – 6:00 p.m. **Registration:** Pick up badges & handout (*Dining Room Lounge*). Please lunch before arriving. (No lunch will be served at the camp.)
- 1:00 – 8:00 p.m. **Lodge check-in:** Get room assignment, room key, information, and map of lodge area.
If physically challenged, please notify desk of special needs.
- 1:30 – 3:30 p.m. Tutorial #1: “Theory and application of non-contact methods for in-line reliability determination” by John D’Amico, Semiconductor Diagnostics, Inc.
- 3:30 – 4:00 p.m. Break
- 4:00 – 6:00 p.m. Tutorial #2: “Fast wafer level reliability monitoring of product wafers” by Andreas Martin, Infineon Technologies
- 6:00 – 7:30 p.m. DINNER, (*Dining Room*) Introduction of workshop agenda; dine with your session chair
- 7:30 – 8:30 p.m. Tutorial # 3: “MRAM and reliability” by Brian Hughes, Infineon Technologies
- 8:30 – 9:00 p.m. Discussion Group Assignments/SIG signup (*Dining Room Lounge*); Poster Preparation (*Old Lodge*)
- 9:00 – 10:30 p.m. Mixer & Poster Session 1, (*Cathedral Room*)

TUESDAY, October 21

- 7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)
- 8:15 – 8:30 a.m. Welcome & Introduction: Gennadi Bersuker, General Chair. Program Overview: Alvin W. Strong, Tech. Prog. Chair (*Angora Rm.*)
- 8:30 – 9:30 a.m. Keynote: “The complete metrology roadmap” by Alain C. Diebold, International SEMATECH
- 9:30 – 9:45 a.m. Break
- 9:45 – 11:25 a.m. Session #1: GATE DIELECTRICS – SiO₂
- 1.1. Interface traps and oxide traps creation under NBTI and PBTI in advanced CMOS technology with a 2 nm gate-oxide—M. Denais, STMicroelectronics/L2MP-ISEM, V. Huard, Philips Semiconductors, C. Parthasarathy, STMicroelectronics, G. Ribes, STMicroelectronics/IMEP/ENSERG, F. Perrier, Philips Semiconductors, N. Revil, STMicroelectronics, and A. Bravaix, L2MP-ISEM
 - 1.2. Non-invasive nature of corona charging on thermal Si/SiO₂ structures—M. Dautrich, P.M. Lenahan, A.Y. Kang, Penn State University, and J.F. Conley, Jr., Sharp Labs of America
 - 1.3. Gate oxide reliability parameters in the range 1.6 to 10 nm—R.-P. Vollertsen, Infineon Technologies AG and E.Y. Wu, IBM Microelectronics
 - 1.4. PMOS NBTI-induced circuit mismatch in advanced technologies—M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H.S. Muthali and S. Jacobs, Intel Corporation
- 11:25 – 12:00 p.m. Group Picture
- 12:00 – 1:30 p.m. LUNCH, *Dining Room*
- 1:30 – 3:30 p.m. Tutorial 4: “Reliability physics and chemistry of thin and high-k gate oxides” by Pat Lenahan, Penn State University
- 3:30 – 4:00 p.m. Break
- 4:00 – 5:15 p.m. Session #2: GATE DIELECTRICS – HIGH-K
- 2.1. Stress test and characterization of high-k thin films—W. Luo, D. Sunard, Y. Kuo, W. Kuo, Texas A&M University
 - 2.2. Reliability concerns for HfO₂/Si devices: dielectric electron traps—A.Y. Kang, P.M. Lenahan, Penn State University, J.F. Conley, Jr., and Y. Ono, Sharp Labs of America
 - 2.3. Charge trapping in MOCVD hafnium-based gate dielectric stack structures and the impact on device performance—C.D. Young, G. Bersuker, G.A. Brown, C. Lim, P. Lysaght, P. Zeitzoff, R.W. Murto, and H.R. Huff, International SEMATECH
 - 2.4. Product specific sub-micron E-Fuse reliability and design qualification—W.R. Tonti, J.A. Fifield, J. Higgins, W. Guthrie, W. Berry, C. Narayan, IBM
- 6:00 – 7:30 p.m. DINNER, *Dining Room*
- 7:30 – 9:00 p.m. Poster Session 2
- 9:00 – 9:45 p.m. Discussion Groups.; Chair: *Sylvie Bruyere, STMicroelectronics* (45 minute parallel sessions for each topic)
Attendees are to participate in one of the groups
- 9:45 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

WEDNESDAY, October 22

- 7:00 – 8:00 a.m. BREAKFAST (*Dinning Room*)
- 8:00 – 8:10 a.m. Announcements, (*Angora Room*)
- 8:10 – 10:15 a.m. Session #3: BIP
- 3.1. Projecting the reliability of SiGe NPN transistors after AC Ube reverse stress from DC device lifetime—K. Hofmann, Infineon Technologies AG
 - 3.2. A current mirror method for thermal instability of SOI BJT—J. Kim, Y. Liu, and J.A De Santis, National Semiconductor Corporation
 - 3.3. DC and AC hot-carrier characteristics of ultra-thin DPN gate dielectric on partially depleted SOI MOSFETs—E. Zhao, J. Chan, J. Zhang, A.P. Marathe, and K.O. Taylor, AMD

- 3.4. Performance-reliability trade-offs in high speed Si-Ge BiCMOS—B. O'Connell, P. Chaparala, and B. Mehrotra, National Semiconductor Corporation
- 3.5. Breakdown walk-in a new PMOS failure mode in high power BiCMOS applications—D.J. Brisbin, A. Strachan, and P. Chaparala, National Semiconductor Corporation

10:15 – 10:45 a.m. Break

10:45 – 12:00 p.m. Session #4: CIRCUITS

- 4.1. Using time-dependent reliability fallout as a function of yield to optimize burn-in time for a 130 nm SRAM device—K.R. Forbes and N. Arguello, Motorola Semiconductor Product Sector
- 4.2. Leakage current recovery in SRAM after AC stressing—C. Payan, S. Kumar, A. Thupil, Cypress Semiconductor, S. Kasichainula, Extreme Networks, and W.B. Knowlton, Boise State University
- 4.3. Effects of circuit-level stress on inverter performance and MOSFET characteristics—N. Stutzke, B.J. Cheek, M. Wiscombe, T. Lowman, Boise State University, S. Kumar, Cypress Semiconductor, R.J. Baker, A.J. Moll, and W.B. Knowlton, Boise State University

12:00 – 1:30 p.m. LUNCH, (*Dining Room* — Take out Lunch bags available)

1:30 – 6:00 p.m. Open: The afternoon is free for discussion, hiking & other recreation; or for viewing videos shown in parallel:

- (1) Oxide wearout/breakdown/reliability (*Angora Room*)
- (2) MEMS performance and reliability (*Cathedral Room*)
- (3) Accelerated stress testing (*TBA*)

6:00 – 7:30 p.m. DINNER, (*Dining Room*)

7:30 – 9:00 p.m. Discussion Groups,; Chair: *Sylvie Bruyere, STMicroelectronics* (90 minute parallel sessions for each topic)

9:00 – 10:30 p.m. Individual SIG Meetings

THURSDAY, October 23

7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)

8:15 – 8:30 a.m. Announcements, (*Angora Room*)

8:30 – 10:10 a.m. Session 5 INTERCONNECT/MEMORY

- 5.1. Physically-based simulation of the early and long-term failures in the copper dual-damascene interconnect—V. Sukharev, R. Choudhury, and C.W. Park, LSI Logic Corporation
- 5.2. Dielectric reliability studies of Metal Insulator Metal Capacitors (MIMCAP) with SiN dielectric under unipolar to bipolar AC-stress—R. Schwab and K.H. Allers, Infineon Technologies AG
- 5.3. A reliability evaluation methodology for memory chips for space applications when sample size is small—Y. Chen, D. Nguyen, S. Guertin, Jet Propulsion Lab, J. Bernstein, University of Maryland, M. White, R. Menke, and S. Kayali, Jet Propulsion Lab
- 5.4. Improvement of write/erase cycling of memory cells with SiO₂/HfO₂ tunnel dielectric—P. Blomme, B. Govoreanu, IMEC/KULeuven, J. Van Houdt, IMEC, and K. De Meyer, IMEC/KULeuven,

10:10 – 10:40 a.m. Break

10:40 – 11:40 p.m. Wrap-Up

11:45 – 1:15 p.m. LUNCH, (*Dining Room*)—Leave the Stanford Sierra Camp unless attending JC14.2

2:00 p.m. JEDEC 14.2 Committee on Wafer Level Reliability Meeting

2003 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 23-24)

Meeting registration automatically includes a room reservation.

(Please type, print or attach business card)

NAME: _____
Last First Initial

COMPANY: _____
Mail Stop

ADDRESS: _____

City State/Country Zip/Postal Code

Phone: (_____) _____ Fax: _____

Email: _____

For cabin assignments: male female

Address is HOME

Please check here if you do not wish to receive mail other than from IRW & IRPS

Please check here if physically challenged and you require any auxiliary aids or services.
 Please call (315) 339-3968.

Will bring poster. Title: _____

I am interested in the following Discussion Group(s):

WLR and EM; Ultra-thin and high-K dielectrics;

Other _____

Method of Payment: Check: Make checks payable to: **2003 IEEE/IRW**
 Credit Card: AMEX MASTER CARD VISA Diners Club

Card No.

Expiration Date

Signature

ADVANCE REGISTRATION FEES

IEEE Member (incl. mem# _____) **\$995*** _____

NON-IEEE Member **\$1045*** _____

Sponsored IEEE STUDENT** **\$645*** _____

*Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday—lunch Thursday), Final Workshop Report with CD.

**To promote student involvement at IRW, this year, we will be offering a reduced registration fee of \$645 to the first 15 students who register early. Each reduced rate student registration must be accompanied by a full fee paying professor or sponsor. A professor may sponsor up to three students. Students accepting the discount must either be an IEEE member, or join the IEEE as a student member. SPONSORNAME: _____

EXTRA COPIES of Workshop?

Final Report (printed) Qty: ___ x **\$80** _____

Final Report (CD) ... Qty: ___ x **\$80** _____

Final Report (printed & CD) Qty: ___ x **\$130** _____

JC-14.2 Mtg. accommodations*** **\$200** _____

*** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday—lunch Friday)

TOTAL REMITTED \$ _____

Cancellation fees: \$50 after Sept. 26 ;
 full fee after Oct. 10

Send this completed form and payment to: IRW Registration; P.O. Box 308; Westmoreland, NY 13490 Paying by credit card... fax to 315-336-9134
 Questions? becky@sar101.com or 315-339-3968 or web site: <http://www.irps.org/irw>

REFEREED & OPEN POSTER SESSIONS

Chair: Bill Tonti, IBM Engineering & Technology Services

(Monday & Tuesday Evening)

There are 16 accepted posters (listed below). They cover: hot carriers, negative bias temperature instability, interconnect reliability, and fast gate oxide wafer reliability methodologies. Each refereed poster author will deliver an oral presentation on their results during the poster sessions.

In addition to the already accepted posters *all IRW* attendees are invited to bring a walk-in poster to communicate and discuss their reliability work in progress, or late breaking results. This is a great opportunity to obtain feedback and perhaps collaborate with your peers. Please indicate on the registration form your intention to bring a walk in poster by reserving a poster display board. In addition, you are invited to submit a paper of your poster presentation for inclusion in the Workshop Final Report.

Additional information can be found at:

<http://www.irps.org/irw/poster/>.

- P1 Reliability of dielectric barriers in copper damascene applications—A. Lee, A. Lakshmanan, N. Rajagopalan, Z. Cui, M. Le, L.Q. Xia, B.H. Kim, and H. M'Saad, Applied Materials
- P2 Latch-up failure path between power pins in the mixed-voltage process—C.-N. Wu, H.-M. Chou, and M. Chang, TSMC
- P3 Effect of reverse measurement on the HC instability evaluation of MOSFETs—H. Katto, M. Miyauchi, and Y. Higuchi, Tokyo University of Science
- P4 NBTI mechanism explored on the back gate bias for pMOSFETs—M.-G. Chen, J.-S. Li, C. Jiang, C.H. Liu, K.-C. Su, and Y.-J. Chang, United Microelectronics Corp.
- P5 A design technique to reduce hot carrier effect—E. Xiao, University of Texas at Arlington
- P6 Determination of the maximum voltage for a product screening stress without jeopardizing the product lifetime, based on wafer level TDDDB and HC measurements—H.-H. Kuge, Philips Semiconductor
- P7 Calculations of electronic and elastic properties of Cu-interconnects—Y.N. Shunin, K. Budilov, Information System Institute & Transport and Telecommunication Institute, Y. Zhukovskii, University of Latvia, G. Borstel and O. Sychev, Univ. Osnabrück
- P8 Effect of joule heating on the determination of electromigration—X. Federspiel, Philips Semiconductors, V. Girault, and D. Ney, STM
- P9 Correlation of ramped current to constant voltage gate oxide reliability testing on leading edge DRAM technology—G. Aichmayr and A. Beyer, Infineon Technologies
- P10 Effect of nitrogen incorporation on PMOS negative bias temperature instability in ultra-thin oxy-nitrides—L. Duong, V. Gopinath, S. Prasad, J. Lin, E. Li, and V. Hornback, LSI Logic Corporation
- P11 Effect of new inter-layer-dielectric on plasma charging damage in 0.13 μm dual gate oxide—W.H. Lu, L.H. Ko, K.L.Y. Andrew, and K.F. Lo, Chartered Semiconductor Mfg. Ltd.
- P12 Impact of junction temperature on microelectronic device reliability and considerations for space applications—M. White, M. Cooper, and Y. Chen, JPL
- P13 Massively parallel GOI test—T.K. Ng, K.F. Lo, B.B. Jie and Y. Andrew, Chartered Semiconductor Mfg. Ltd.
- P14 Reliability results on a 0.25 micron aluminum backend with a TiN Liner—L. Westergard, M. Nelson, B. Williams, and J. Prasad, AMI Semiconductor
- P15 HCI lifetime enhancement by PLDD implant energy optimization of Pch MOSFET in 0.13 μm CMOS technology—L. Hyeokjae, E. Quek, Y. Andrew and M. Fakhru Karim, Chartered Semiconductor Mfg. Ltd.
- P16 Similarity of Pre-Breakdown Leakage Current Fluctuations for p- and nMOSFETs—J.C. Reiner, EMPA

DISCUSSION GROUPS

Chair: Sylvie Bruyere, STMicroelectronics

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of at least two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of leaders who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp.

SPECIAL INTEREST GROUPS

Chair: Sylvie Bruyere, STMicroelectronics

The Special Interest Groups (SIGs) program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information on SIGs see <http://www.irps.org/irw/sig/>.

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

JEDEC 14.2 MEETING. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is \$200, which includes Thursday night dinner and lodging and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org, or call Mike Dion, JC-14.2 Chair at (321) 724-7067.

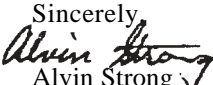
QUESTIONS? If you have any questions, please contact either: Technical Program Chair, Alvin Strong, by phone, (802) 769-1326, fax..4287, or email: astrong@us.ibm.com; Technical Program Vice Chair, Rolf Vollertsen by email: rolf.vollertsen@infineon.com; or General Chair, Gennadi Bersuker, by phone (512) 356-7045, email: gennadi.bersuker@sematech.org.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. Space at the Camp limits IRW to approximately 120 attendees.

We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions.

We look forward to seeing you at the Workshop!

Sincerely,

Alvin Strong
Technical Program Chair

ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- All participants must stay at the camp during the workshop.
- We cannot accommodate spouses or any companions at the camp.
- Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.
- Smoking is permitted outdoors only. Smoking is not permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls, (530) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.

TRAVEL ARRANGEMENTS

Special discounted airfares for IRW have been negotiated by IEEE Global Travel Services. Please note that this service can be used by attendees traveling from within or outside of the United States and Canada. Discounts are as high as 20% off the lowest published airfares with American, TWA, Continental and United airlines. Special rates have also been negotiated with Avis Rental Car Company. Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Global Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call 800-879-4333; and outside of the US and Canada, call +1 732-562-5387. Or, visit their on-line travel service web site at www.ieeetravelonline.org. At this secure site you can search, reserve, and ticket your travel anytime, anywhere. You may also fax your requirements to the IEEE Global Travel Services at 732-562-8815. When faxing, please be sure to include your travel dates, departure, return times, phone and fax numbers and mention the IEEE IRW. A Travel Counselor will contact you promptly.

TRANSPORTATION TO THE CAMP. The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from the Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the **Tahoe Casino Express** (\$19 or \$34 roundtrip). For Tahoe Casino Express schedule details call 800-446-6128, or go <http://www.tahoecasinoexpress.com>.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 20). Return trips to the Casino are offered on the last day of the conference only. If you are planning on **using the Casino Express**, please notify Stanford Sierra Camp (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the camp at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino.

